ABSTRACT

In a standard Flash EPROM, a plurality of flash memory cells are arranged in an array of rows and columns. In order to determine the programming state of each cell, the magnitude of the cell read current is measured using a reference current source set to approximately 25uA. The memory cell being examined is connected with the drain wired to a positive voltage between about 1 to 2 volts. The source of the memory cell is connected to the current source. The control gate voltage is set to approximately 5V. An unprogrammed memory cell will have a drain current equal to that of the reference current source and the cell output will be slightly less than the drain voltage (logic 1). Under these conditions, a programmed memory cell, having a higher threshold voltage, will conduct only leakage currents. This results in the cell output being very close to ground potential (logic 0). Older technologies utilized fixed current sources for the reference current. In order to better track manufacturing tolerances, more recent technologies use a "reference cell" identical to the standard memory cell to form the reference current source. This reference cell is erased under the same conditions as a memory cell. Since the memory and reference cells are identical in geometry, their current characteristics will track regardless of manufacturing process variations. In order to maintain the proper state for the reference cells, they must be periodically erased. Most manufacturers erase the reference cells during a mass erase resulting in repeated high voltage stress equal to the memory array and decoder. The present invention reduces this high voltage stress using a method where a pulse initiating the erasure of the reference cells is generated upon application of power to the memory.